REMARKS

None of the claims are amended hereby. No claims are added or canceled. Accordingly, after entry of this response, claims 1-26 and 28-44 will remain pending.

This response is being presented together with a Request for Continued Examination so that the Examiner may consider the remarks that follow.

In the Final Office Action dated September 13, 2005, the Examiner rejected claims 1-4, 6-21, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Niimi et al. (U.S. Patent No. 6,503,846). Claims 24-26 and 28-29 were rejected under 35 U.S.C. § 103(a) as unpatentable over Niimi et al. in view of Park et al. (U.S. Patent No. 6,825,518). Next, claim 30 was rejected under 35 U.S.C. § 103(a) as unpatentable over Niimi et al. in view of Subramony et al. (U.S. Patent Application Publication No. 2003/0138562). In addition, the Examiner rejected claims 31-42 under 35 U.S.C. § 103(a) as unpatentable over Niimi et al. and Subramony et al. in view of Ikakura et al. (U.S. Patent No. 6,255,230). The Examiner also rejected claims 5 and 22 under 35 U.S.C. § 103(a) as unpatentable over Niimi et al. in view of Solayappan et al. (U.S. Patent No. 5,997,642). Further, claims 43-44 were rejected under 35 U.S.C. § 103(a) as unpatentable over Niimi et al. and Subramony et al. in view of Solayappan et al. The Applicant respectfully disagrees with each of these rejections and respectfully requests that the Examiner consider the following remarks in response to these rejections.

As noted in the response filed on July 20, 2005, the prior art does not describe or suggest a method or processing system that creates an oxynitride layer in the absence of a plasma.

Niimi et al. describes the use of a temperature spike for uniform nitridation of ultra-thin silicon dioxide layers in transistor gates. The substrate 101, which is

preferably a silicon substrate, has a surface 102 with an insulating layer 103 thereon. (Niimi et al. at col. 4, lines 15-20.) The insulating layer 103, which is preferably silicon dioxide, is grown by rapid thermal oxidation in a furnace. (Niimi et al. at col. 4, lines 20-24.)

Fig. 2 of Niimi et al. illustrates the process step 204 of plasma nitridation of the insulating layer 103. (Niimi et al. at col. 4, lines 30-31.) Nitridation occurs by exposing the insulating layer 103 to a nitrogen-containing plasma. (Niimi et al. at col.. 4, lines 30-49; see also Niimi et al. at col. 5, lines 52-56.) At no point does Niimi et al. describe nitridation of the insulating layer 103 by any other process, nor would those skilled in the art understand Niimi et al. to describe any other process. Every embodiment described by Niimi et al. relies on a nitrogen-containing plasma for nitridation. Accordingly, Niimi et al. does not describe or suggest a method or a processing system relying on a self-limiting, thermal oxidation process.

At the top of page 3 of the September Final Office Action, the Examiner recognized that Niimi et al. does not describe or suggest a method or a processing system with a self-limiting, thermal oxidation process. To find this suggestion, the Examiner pointed to col. 5, lines 52-56, of Niimi et al. The Applicant has reviewed this section in Niimi et al. and respectfully disagrees with its application to the claims of the present invention. As the Applicant understands the portion from Niimi et al. to which the Examiner refers, that section concerns **plasma nitridation**. (See, e.g, Niimi et al. at col. 5, lines 45-46.) Moreover, All of the portions of Niimi et al. that discuss process parameters for nitridation do so in connection with a discussion of **plasma nitridation**. Accordingly, that Applicant respectfully submits that Niimi et al. is not applicable to the present invention.

Park et al., Subramony et al., Ikakura et al., and Solayappan et al. do not assist the Examiner in rejecting the claims, because these references fail to cure the deficiencies noted with respect to Niimi et al.

Park et al. describes a capacitor in a semiconductor device and method for fabricating the capacitor. Specifically, a silicon nitride layer 3 is formed on the lower (silicon) electrode 2. (Park et al. at col. 3, lines 40-45.) The silicon nitride layer 3 may be formed by a nitridation process using a plasma NH_3 treatment, a nitridation process using a thermal NH_3 treatment, or an N-LPCVD process. (Park et al. at col. 3, lines 45-50.) After the nitridation process, an oxidation treatment is performed to form the a silicon oxynitride layer 4 on the surface of the silicon nitride layer 3. (Park et al. at col. 3, lines 51-54.) There is no discussion of flowing a process gas comprising a nitrogen-containing oxidizing gas in the process chamber nor is there any discussion of forming an oxynitride layer on the substrate, the oxynitride layer being formed in a self-limiting, thermal oxidation process. As a result, the Applicant respectfully submits that Park et al. cannot be combined properly with Niimi et al. to render obvious any of the claims presented by the above-captioned application.

As discussed in the July 2005 Amendment, Subramony et al. describes methods for silicon oxide and oxynitride deposition using single wafer low pressure CVD. To create an oxynitride layer, Subramony et al. introduces both a silicon-containing gas and a nitrogen containing gas into the reaction chamber 490. (Subramony et al. at paragraphs [0075] and [0076].) The reactant gases are thermally decomposed to form the oxide or oxynitride for deposition on the surface of the substrate 300. (Subramony et al. at paragraphs [0062] - [0064] and [0077] –[0079].) No where, however, does Subramony et al. describe a self-limiting, thermal oxidation process for the creation of an oxynitride layer. Accordingly, contrary to the

Examiner's assertion, Subramony et al. cannot be properly combined with the remaining references to render obvious any of the claims.

Ikakura et al. does not assist the Examiner with the rejection of any of the claims, because Ikakura et al. does not cure the deficiencies noted with respect to Niimi et al. Park et al., or Subramony et al. Ikakura et al. describes a method of modifying a film forming surface of a substrate on which a film is to be formed. Prior to a CVD step (*e.g.*, the CVD process of Subramony et al.), Ikakura et al. describes modification of the surface of a silicon dioxide film, a silicon nitride film, or the like. (Ikakura et al. at col. 1, lines 11-20, and col. 4, lines 54-67.) No where does Ikakura et al. describe or suggest a self-limiting, thermal oxidation process as recited by the claims.

Solayappan et al. does not assist the Examiner with the rejection of any of the claims, because Solayappan et al. describes a method and apparatus for misted deposition of integrated circuit quality thin films. The film is formed from a liquid precursor, such as strontium bismuth tantalate. (Solayappan et al. at col. 7, lines 33-44.) No where does Solayappan et al. discuss at least a self-limiting thermal oxidation process for the formation of an oxynitride layer. Accordingly, the reference cannot be properly combined to render the claims unpatentable.

Each of the rejections asserted by the Examiner having been addressed, the Applicant respectfully submits that claims 1-26 and 28-44 are patentable over the references cited by the Examiner. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejections asserted against claims 1-26 and 28-44 and pass this application quickly to issue.

If the Examiner believes a telephone conference would be helpful, he is invited to contact the undersigned at the telephone number given below.

Respectfully submitted,

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